ABSTRACT OF THE DISCLOSURE

A self refresh timer is set constantly to an operation state to render a refresh request signal FAY active periodically. When contention occurs between the refresh request signal FAY and an externally applied read or write command, a row selection related circuit/command generation related circuit controls a row related control signal so that a refresh operation is carried out after, for example, the read or write operation ends. A submemory array SMA is divided more small than that of the conventional case, and the refresh cycle ends in a shorter period of time. Therefore, a read operation and a refresh operation can be completed within a read cycle time. A DRAM core that can be employed with control as simple as that of an SRAM can be realized.